Low Temperature Characterization of FD-SOI Transistors for Extreme Environments in Deep Space exploration Missions

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Abstract:

Fully depleted silicon on insulator (FD-SOI) technology is an extremely attractive candidate for future low power and high speed electronic systems because it offers increased transconductance, decreased sub-threshold slope, reduced short channel effects, elimination of kink effect and enhanced low field mobility. These benefits can be applied to deep space exploration in extreme environments once the characterization is done at low temperatures with the addition of the space radiation effects. From this characterization, it would also be possible to make essential changes for a better performing and more survivable FD-SOI technology in extreme space environments.

FD-SOI transistors (P and N type) with channel lengths of 0.25, 0.30 and 0.35 microns were characterized at variable low temperatures in the range of 79K to 300K. Interesting changes in device characteristics resulting from the temperature dependence of channel mobility, threshold voltage, and effective channel length in both P and N transistors are compared for the three feature lengths. Results are extremely useful in determining the survivability and performance of FD-SOI circuits in extreme environments over a prolonged period of operation such as in deep space exploration missions. Results also provide insight into the selection of a proper technology for better performance in low temperature applications. Device simulator ISE-DESSIS is used for simulating variable temperature (low) effects on device parameters and their remediation through changes in device architecture, device geometry, and doping concentrations and profiles. Such simulations also help the verification of the fabrication quality and consistency of given test structures.

We have observed an increase in threshold voltage (Vth) with decreasing temperature in the range from 300K to 150K. Below 100K, Vth starts to decrease with temperature. This behavior has been verified using three different methods for the extraction of the threshold voltage. However, although Vth increases, we also observed that the overall current increases as temperature decreases. The observations are easily explained as we examine the behavior of the effective mobility in that temperature range. We have used the following equation:

$$\mu_{eff} = \frac{Id}{(W/L)QiVds} \quad \text{Where } Qi = C_{ox}(V_g - V_t)$$

By using this method, effective mobility is more accurate for experimental gate voltages above Vth. Effective mobility was found to increase with decreasing temperature when reasonably high gate voltages are applied. This effect has sufficiently countered the increasing trend of Vth to yield an overall inversely proportional relationship between current and temperature.

An interesting result is the variation of the effective mobility with channel length at a given temperature. It was found that the effective mobility is the highest for 0.3 micron channel length transistors. The effective mobility is nearly the same for both 0.25 and 0.35 micron transistors.

The variation in transconductance as a function of the gate voltage across different temperatures also confirms the combination of mobility and threshold voltage behaviors. The transconductance was found to increase when the temperature decreases from 300K to 150K, and it decreased for decreasing temperatures below 100K.